What is claimed is:

1. A method for fabricating a power semiconductor device comprising:

sequentially forming an epitaxial layer of a first conductivity type having a low concentration and a body region of a second conductivity type on a semiconductor substrate of the first conductivity type having a high concentration;

forming an oxide layer pattern on the body region;

forming a first trench using the oxide layer pattern as an etching mask to perforate a predetermined portion of the body region having a first thickness;

forming a body contact region of the second conductivity type having a high concentration to surround the first trench by impurity ion implantation using the oxide layer pattern as an ion implantation mask;

forming first spacer layers to cover the sidewalls of the first trench and the sidewalls of the oxide layer pattern;

forming a second trench using the oxide layer pattern and the first spacer layers as etching masks to perforate a predetermined portion of the body region having a second thickness greater than the first thickness;

forming a source region of the first conductivity type having a high concentration to surround the second trench by impurity ion implantation using the oxide layer pattern and the first spacer layers as ion implantation masks;

forming second spacer layers to cover the sidewalls of the second trench and the sidewalls of the first spacer layers;

forming a third trench to a predetermined depth of the epitaxial layer using the oxide layer pattern, the first spacer layers, and the second spacer layers as etching masks;

forming a gate insulating layer in the third trench;

forming a gate conductive pattern in the gate insulating layer;

forming an oxide layer on the gate conductive layer pattern;

removing the first and second spacer layers;

forming a first metal electrode layer to be electrically connected to the source region and the body contact region;

forming a second metal electrode layer to be electrically connected to the gate conductive layer pattern; and

forming a third metal electrode layer to be electrically connected to the semiconductor substrate.

2. The method of claim 1, wherein the silicon oxide layer pattern is formed to a thickness of about 4500 Å at a temperature of about 1000 °C.

3. The method of claim 1, wherein forming the first spacer layers comprises:

forming a material layer to cover the first trench and the silicon oxide layer pattern; and

etching back the material layer.

4. The method of claim 1, wherein forming the second spacer layers comprises:

forming a material layer to cover the second trench, the first spacer layers, and the silicon oxide layer pattern; and

etching back the material layer.

5. The method of claim 3 or 4, wherein the material layer used to form the first or second spacer layers is a nitride layer.

6. The method of claim 3 or 4, wherein the material layer used to form the first or second spacer layers is formed by low pressure chemical vapor deposition.

7. The method of claim 3 or 4, wherein etching the material layer is performed by plasma ion etching.

8. The method of claim 1, wherein the first conductivity type is an n-type, and the second conductivity type is a p-type.

9. The method of claim 1, wherein the first conductivity type is a p-type, and the second conductivity type is an n-type.